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EXAMINER	
VIGUSHIN, JOHN B	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 09/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,640	BRAND ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8 and 16-18* is/are allowed.

6)☒ Claim(s) *1-4,6,7,9,10 and 12-15* is/are rejected.

7)☒ Claim(s) *5,11 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 13 is objected to because of the following informalities:

In Claim 13, line 3 of the final paragraph lacks a subject for the phrase "is contacted to the connector pins....". *What* is "contacted to the connector pins?" This problem can be easily fixed by inserting --the at least one blocking capacitor-- before "is" in line 3 of the final paragraph of the claim.

Appropriate correction is required.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Searls et al. (US 2003/0218235 A1)

Blasi et al. (US 5,973,928)

Haller et al. (US 5,077,639)

Hernandez et al. (US 4,734,818)

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Searls et al.

As to Claim 1, Searls et al. discloses, in Figs. 2, 2A and 7: an integrated circuit (224, 724; see paragraphs [0019] and [0034]), having a housing (i.e., die 226, 726 mounted on a package substrate 228, 724) with a plurality of connector pins (214, 238; and 714, 738, 760, 762); a printed circuit board (212, 712) having conductive paths, to which the integrated circuit (224, 710) is electrically and mechanically contacted by connector pins (214, 238; and 714, 738, 760, 762); at least one blocking capacitor (230; and 730A, 730B, 730C), which is switched into a power supply path for the integrated circuit 710 (see paragraphs [0029], [0034] and [0055]), wherein the at least one blocking capacitor (230; and 730A, 730B, 730C) is spatially arranged between the connector pins (i.e., between pins 214, 238; and between pins 714, 738, 760, 762) of the housing and is electrically contacted to the connector pins (i.e., electrically contacted to pins 214, 238; and to pins 714, 738, 760, 762; see paragraphs [0035] and [0055]).

As to Claim 2, Searls et al. further discloses the integrated circuit (224, 724) has a ball grid array housing with ball-shaped connector pins (214, 238; and 714, 738, 760, 762).

As to Claim 13, Searls et al. discloses, in Figs. 2, 2A and 7: arranging the at least one blocking capacitor (230; and 730A, 730B, 730C) in a current supply path for an integrated circuit 224, 724), having a housing (i.e., die 226, 726 mounted on a package substrate 228, 724) with a plurality of connector pins (214, 238; and 714, 738, 760, 762), which are electrically and mechanically contacted to conducting paths of a printed

circuit board (212, 712) arranged in proximity to the housing; and spatially arranging the at least one blocking capacitor (230; and 730A, 730B, 730C) between the printed circuit board (212, 712) and the integrated circuit (224, 724), and the at least one blocking capacitor (230; and 730A, 730B, 730C) is contacted to the connector pins (214, 238; and 714, 738, 760, 762) of the housing of the integrated circuit (224, 724) (i.e., electrically contacted to pins 214, 238; and to pins 714, 738, 760, 762; see paragraphs [0035] and [0055]).

5. Claims 1 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Hernandez et al.

As to Claim 1, Hernandez et al. discloses, in Figs. 10A and 10B: an integrated circuit 64, having a housing with a plurality of connector pins 66; a printed circuit board 68 having conductive paths, to which the integrated circuit 64 is electrically and mechanically contacted by connector pins 66; at least one blocking capacitor 60, which is switched into a power supply path for the integrated circuit (Figs. 8A,B; col.6: 52-col.7: 4), wherein the at least one blocking capacitor 60 is spatially arranged between the connector pins 66 of the housing and is electrically contacted to the connector pins 66 (col.7: 31-40).

As to Claim 13, Hernandez et al. discloses, in Figs. 10A and 10B: arranging the at least one blocking capacitor 60 in a current supply path for an integrated circuit 64, having a housing with a plurality of connector pins 66 (Figs. 8A,B; col.6: 52-col.7: 4), which are electrically and mechanically contacted to conducting paths of a printed circuit board 68 arranged in proximity to the housing (col.7: 31-40); and spatially arranging the

at least one blocking capacitor between the printed circuit board 68 and the integrated circuit 64, and the at least one blocking capacitor 60 is contacted to the connector pins 66 of the housing of the integrated circuit 64 (col.7: 31-40).

6. Claims 1 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Blasi et al.

As to Claim 1, Blasi et al. discloses, in Fig. 4: an integrated circuit, having a housing 40 with a plurality of connector pins 44; a printed circuit board 45 having conductive paths, to which the integrated circuit is electrically and mechanically contacted by connector pins 44 (col.3: 17-22); at least one blocking capacitor 41, which is switched into a power supply path for the integrated circuit (col.1: 18-21; col.2: 49-56), wherein the at least one blocking capacitor 41 is spatially arranged between the connector pins 44 of the housing 40 and electrically--*indirectly* through the inner wiring only and *not directly externally*--contacted to the connector pins 44 (col.2: 31-39 and 49-56).

As to Claim 13, Blasi et al. discloses, in Fig. 4: arranging the at least one blocking capacitor 41 in a current supply path for an integrated circuit 42 (col.1: 18-21; col.2: 49-56), having a housing 40 with a plurality of connector pins 44, which are electrically and mechanically contacted to conducting paths of a printed circuit board 45 arranged in proximity to the housing 40; and spatially arranging the at least one blocking capacitor 41 between the printed circuit board 45 and the integrated circuit 42, and the at least one blocking capacitor 41 is contacted--*indirectly* through the inner wiring only

and *not directly externally*-- to the connector pins 44 of the housing 40 of the integrated circuit 42 (col.2: 31-39 and 49-56).

7. Claims 1, 3, 4, 6, 7, 9 and 12-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Haller et al.

As to Claim 1, Haller et al. discloses, in Fig. 5: an integrated circuit 10, having a housing with a plurality of connector pins 11; a printed circuit board 13 having conducting paths, to which the integrated circuit 10 is electrically and mechanically contacted by connector pins 11 (col.4: 23-25); at least one blocking capacitor 7 (col.1: 10-15), which is switched into a power supply path for the integrated circuit 10 (col.3: 49-50 and col.4: 10-13); the blocking capacitor 7, of which there is at least one, is spatially arranged between the connector pins 11 of the housing (specifically, between the two rows of connector pins 11 of the housing) and is electrically contacted to the connector pins 11 (by way of tracks 3 and 4; col.4: 17-23).

As to Claim 3, Haller et al. further discloses the integrated circuit 10 with the housing, the connector pins 11 of which are inserted through openings 2 of a carrier 1 (Figs. 1 and 5; col.4: 17-21) arranged between the housing (of IC 10) and printed circuit board 13 (Fig. 5).

As to Claim 4, Haller et al. further discloses the openings 2 are in the form of bore holes (Fig. 1 and col.3: 42-45).

As to Claim 6, Haller et al. further discloses the at least one blocking capacitor 7 is positioned on a side of the carrier 1 facing toward the housing (Fig. 5).

As to Claim 7, Haller et al. discloses, in Figs. 1 and 5, a carrier 1 comprising: openings 2, through which connector pins 11 of a housing 10 surrounding an integrated circuit can be inserted; and at least one blocking capacitor 7 (col.1: 10-15), which is mounted on the carrier 1 between openings 2 (col.4: 17-25).

As to Claim 9, Haller et al. further discloses that openings 2 are bore holes (col.3: 42-45).

As to Claim 12, Haller et al. further discloses a carrier 1 comprising openings 2, through which connector pins 11 of a housing surrounding an integrated circuit 10 can be inserted, and at least one blocking capacitor 7, which is mounted on the carrier 1 between the openings 2 (specifically, between the two rows of openings 2), is introduced between the housing of the integrated circuit 10 and the printed circuit board 13 (Fig. 5).

As to Claim 13, Haller et al. discloses, in Fig. 5: arranging at least one blocking capacitor 7 (col.1: 10-15) in a current supply path for an integrated circuit 10, having a housing with a plurality of connector pins 11 (col.3: 49-50 and col.4: 10-13), which are electrically and mechanically contacted to conducting paths of a printed circuit board 13 arranged in proximity to the housing (col.4: 23-25); and spatially arranging the at least one blocking capacitor 7 between the printed circuit board 13 and the integrated circuit 10 and the at least one blocking capacitor 7 is contacted to the connector pins 11 of the housing of the integrated circuit 10 (by way of tracks 3 and 4; col.4: 17-23).

As to Claim 14, Haller et al. further discloses the at least one blocking capacitor 7 is assembled before assembly (of Fig. 5) onto a carrier 1 (Fig. 1; col.3: 39-52) between

openings 2 thereof (specifically, between the two rows of the openings 2 of carrier 1 in Fig. 1).

As to Claim 15, Haller et al. further discloses the connector pins 11 are inserted through the openings 2 of the carrier 1 positioned between the housing and the printed circuit board 13 (Fig. 5; col.4: 17-25).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Haller et al.

Haller et al. discloses that blocking capacitor 7 is a surface-mount-device (SMD) that is surface mounted to the conductor tracks 3 and 4 of carrier 1 (col.3: 49-50) but is silent as to the surface mounting details. However, the Examiner takes official notice that it is old and well-known in the SMD art to bond the device to the circuit board conductors using, for example, solder, conductive adhesives, or welding for the purpose of providing reliable electro-mechanical surface-mounted connections of components onto the circuit substrates, and that it would have been obvious to one of ordinary skill in the art at the time the invention was made to also use a surface mount bonding material--such as a solder or conductive adhesive--or a welding process in order to bond the electrodes of the blocking capacitor 7 to the conductive bonding sites of carrier 1 for the purpose of providing an excellent electrical and mechanical connection of the blocking capacitor to the surface of carrier 1, for which said bonding materials and welds are well-known and widely used in the surface mounting of components to circuit substrates.

Allowable Subject Matter

11. Claims 8 and 16-18 have been allowed.

12. Claims 5, 11 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 5, patentability resides in the limitation wherein *the at least one blocking capacitor is positioned on a side of the carrier facing away from the housing*, in combination with the other limitations of the claim.

As to Claims 8 and 16-18, patentability resides in *the at least one blocking capacitor inserted **into** the carrier between the openings*, in combination with the other limitations of base Claim 8.

As to Claim 11, patentability resides in the limitation wherein *the carrier is made out of a heat-resistant foil*, in combination with the other limitations of the claim.

As to Claim 19, patentability resides in *the at least one blocking capacitor inserted **into** the carrier between the openings*, in combination with the other limitations of the claim.

14. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Werther discloses, in Figs. 4 and 5: an integrated circuit 20, having a housing with a plurality of connector pins 22 (col.9: 47-48); a printed circuit board 10 having conducting paths (col.6: 24-30), to which the integrated circuit 20 is electrically and mechanically contacted by connector pins 14 (of pin carrier 16); at least one blocking

capacitor 58, which is switched into a power supply path for the integrated circuit 20 (Fig. 5 and col.10: 41-52); the at least one blocking capacitor 58 is spatially arranged between the connector pins 14 *of the pin carrier* 16 and not the connector pins 22 of the housing of integrated circuit 20.

b) The following references disclose at least one blocking capacitor that is spatially arranged between the connector pins of the integrated circuit housing and electrically contacted to the connector pins, and further disclose that the at least one blocking capacitor is disposed between the printed circuit board and the integrated circuit housing:

Jodoin (US 4,636,918): IC 10 having housing with connector pins 12; blocking capacitor 20; printed circuit board 14 (Fig. 1).

Lin et al. (US 5,234,198): IC 52 having housing with pins 32; blocking capacitor 50; printed circuit board 38.

Goodwin et al. (US 6,043,987): Figs. 3-6.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
September 22, 2005